REMARKS

Claims 1, 3-8, and 10-18 are pending in the above-identified application. Claims 1, 3, 4, 6, 8, 10, 11, and 13 are independent. Claims 15-18 have been added.

Claim Rejection

Claims 1, 3, 4, 6, 8, 10, 11, and 13 have been rejected under 35 U.S.C. 102(b) as being anticipated by JP 01-223586 of Omichi et al. (referred to as "Omichi"). Applicants respectfully traverse this rejection.

The microcomputer of the present invention includes a boot ROM that enables automatic control of the testing process. The boot ROM contains a control program to operate the communication circuit 14 (Specification at page 14, lines 4-14). In response to receiving a single command from an external communication device (e.g., 20 in Figure 1), the control program sets the conditions necessary for transfer and performs transfer of the test program from the external communication device to the RAM. The control program runs the test program and sends the test results to the external communication device (see Figure 3). Thus, communication between the IC card and the external testing device is initiated by a single command such that the microcomputer automatically performs processes (hence the term "boot ROM"), from the reception

of various test programs to the outputting of test result data. Therefore, the present invention efficiently performs simultaneous testing of a large number of IC cards automatically, because the number of communications to be performed between the IC card and the external testing device is small and the workload on the external testing device is little.

In order to clarify the term "boot ROM" as recited in the claims, independent claims 1, 4, 6, 8, 10, 11, and 13 have been amended to recite that the boot ROM's control program enables receiving of the test program through a communication circuit "in response to receiving a test command" issued by the external check system.

In Omichi, on the other hand, the test program and related commands, etc. are initially received together in a "data block." After the data block is received, programs in the ROM begin operating on the information in the data block. Also, Omichi appears to address removal of the test program after power is turned off, for purposes of security, but does not appear to be concerned with improving communications for efficient testing of a large number of microprocessor devices.

Thus, Applicant submits that Omichi fails to teach or suggest the claimed ROM comprising a control program for enabling receiving of the test program through a communication circuit in response to receiving a test command issued by the external test system.

Similarly, with respect to claim 3, Applicant submits that Omichi fails to teach or suggest the claimed boot ROM having stored a control program for jobs of "receiving a test program for said nonvolatile memory from said check system to be stored in said RAM at a test command issued from said check system."

Accordingly, Applicants submit that Omichi fails to teach or suggest each and every claimed element of claims 1, 3, 4, 6, 8, 10, 11, and 13.

Claim Rejection – 35 U.S.C. 103

Claims 5, 7, 12, and 14 have been rejected under 35 U.S.C. 103 as being unpatentable over Omichi in view of Lin et al. (U.S. Patent 5,818,848, hereinafter "Lin"). Applicants respectfully traverse this rejection.

Lin's integrated circuit uses its I/O port for communication with the external testing device. However, as in the above for Omichi, Lin does not appear to disclose a boot ROM including a control program for enabling receiving a test program from an external check system in response to receiving a test command issued by the external check system. Thus, Applicant submits that Lin does not make up for the above-stated deficiency in Omichi.

Therefore, Omichi and Lin, either alone or in combination, fail to teach or suggest each and every claimed element. Applicants submit that the rejection fails

to establish *prima facie* obviousness and respectfully request that the rejection be withdrawn.

New Claims

New claims 15-18 recite the one-to-many relationship between the test command issued by the control computer and a plurality of microcomputers. For at least the same reasons as in the above for claims 1, 3, 4, and 6, Applicant submits that Omichi and Lin, either alone or in combination, fails to teach each and every element of these claims as well.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1, 3-8, and 10-14 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit

Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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